library ieee;

use ieee.std\_logic\_1164.all;

use ieee.std\_logic\_unsigned.all;

entity ROM is

port(clk: in std\_logic;

addr: in std\_logic\_vector(3 downto 0);

DataOut: out std\_logic\_vector(3 downto 0));

end ROM;

architecture R of ROM is

type Memory is array (15 downto 0) of std\_logic\_vector(3 downto 0);

signal memoryMap: Memory:=("0001","0101","1111","1001","1011","1101","0010","0110","1000","0111","0101","1010","1110","0110","1001","1100");

begin

process(clk)

begin

if clk='1' and clk'event then

DataOut<=memoryMap(conv\_integer(addr));

end if;

end process;

end R;